DS1217M
Nonvolatile Read/Write Cartridge

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GENERAL DESCRIPTION

The DS1217M is a nonvolatile RAM designed for portable applications requiring a rugged and durable package. The nonvolatile cartridge has memory capacities from 64k x 8 to 512k x 8. The cartridge is accessed in continuous 32k byte banks. Bank switching is accomplished under software control by pattern recognition from the address bus. A card edge connector is required for connection to a host system. A standard 30-pin connector can be used for direct mount to a printed circuit board. Alternatively, remote mounting can be accomplished with a ribbon cable terminated with a 28-pin DIP plug. The remote method can be used to retrofit existing systems that have JEDEC 28-pin bytewide memory sites.

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS1217M	0°C to +70°C	30 Cartridge

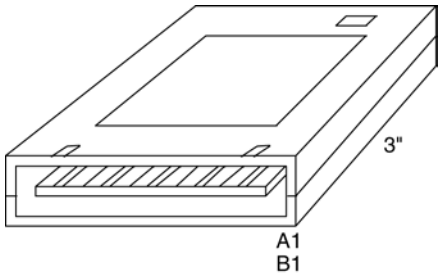
PIN CONFIGURATION

TOP VIEW

Ground	A1	B1	No Connect
+5V	A2	B2	Address 14
$\overline{\text{Write Enable}}$	A3	B3	Address 12
Address 13	A4	B4	Address 7
Address 8	A5	B5	Address 6
Address 9	A6	B6	Address 5
Address 11	A7	B7	Address 4
$\overline{\text{Output Enable}}$	A8	B8	Address 3
Address 10	A9	B9	Address 2
$\overline{\text{Cartridge Enable}}$	A10	B10	Address 1
Data I/O 7	A11	B11	Address 0
Data I/O 6	A12	B12	Data I/O 0
Data I/O 5	A13	B13	Data I/O 1
Data I/O 4	A14	B14	Data I/O 2
Data I/O 3	A15	B15	Ground

FEATURES

- **User Insertable**
- **Data Retention Greater than 5 Years**
- **Capacity to 512k x 8**
- **Standard Bytewide Pinout Facilitates Connection to JEDEC 28-Pin DIP Through Ribbon Cable**
- **Software-Controlled Banks Maintain 32 x 8 JEDEC 28-Pin Compatibility**
- **Multiple Cartridges Can Reside on a Common Bus**
- **Automatic Write Protection Circuitry Safeguards Against Data Loss**
- **Manual Switch Unconditionally Protects Data**
- **Compact Size and Shape**
- **Rugged and Durable**
- **Operating Temperature Range: 0°C to +70°C**



Package Drawing appears at end of data sheet.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Connection Relative to Ground	-0.3V to + 7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-40°C to +70°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}		4.5	5.0	5.5	V
Input High Voltage	V_{IH}		2.2		V_{CC}	V
Input Low Voltage	V_{IL}		0		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IL}		-60		+60	µA
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	I_{IO}		-10		+10	µA
Output Current at 2.4V	I_{OH}		-1.0	-2.0		mA
Output Current at 0.4V	I_{OL}		+2.0	+3.0		mA
Standby Current $\overline{CE}$ = 2.2V	I_{CCS1}			15	25	mA
Operating Current	I_{CCO1}			50	100	mA

CAPACITANCE

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}				100	pF
Input/Output Capacitance	C_{OUT}				100	pF

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = 0°C to +70°C.)

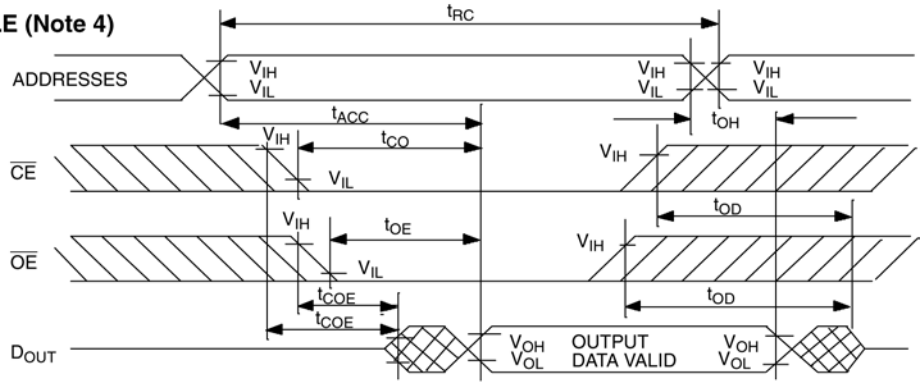
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Read Cycle Time	t_{RC}		250			ns
Access Time	t_{ACC}				250	ns
$\overline{OE}$ to Output Valid	t_{OE}				125	ns
$\overline{CE}$ to Output Valid	t_{CO}				210	ns
$\overline{OE}$ or $\overline{CE}$ to Output Active	t_{COE}	(Note 1)	5			ns
Output High-Z from Deselection	t_{OD}	(Note 1)			125	ns
Output Hold from Address Change	t_{OH}		5			ns
Read Recovery Time	t_{RR}		40			ns
Write Cycle Time	t_{WC}		250			ns
Write Pulse Width	t_{WP}	(Note 2)	170			ns
Address Setup Time	t_{AW}		0			ns
Write Recovery Time	t_{WR}		20			ns
Output High-Z from $\overline{WE}$	t_{ODW}	(Note 1)			100	ns
Output Active from $\overline{WE}$	t_{OEW}	(Note 1)	5			ns
Data Setup Time	t_{DS}	(Note 3)	100			ns
Data Hold Time from $\overline{WE}$	t_{DH}	(Note 3)	20			ns

Note 1: These parameters are sampled with a 5pF load and are not 100% tested.

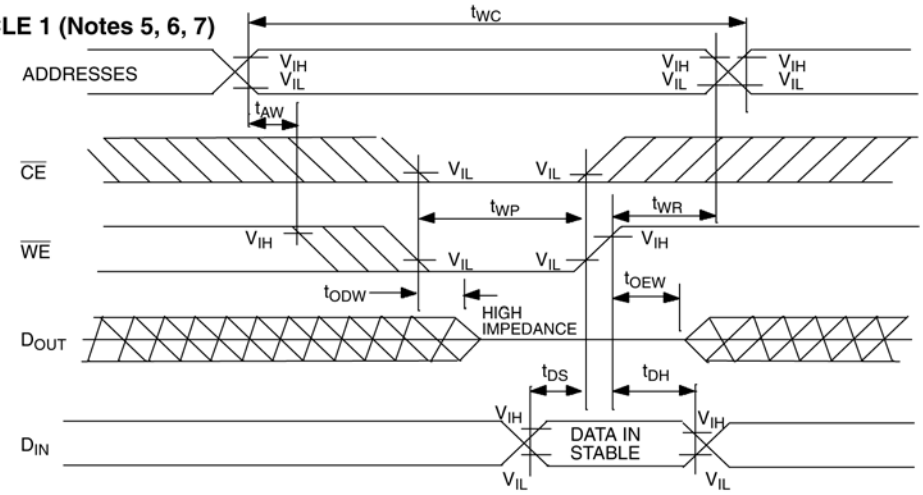
Note 2: t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$ t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

Note 3: t_{DH}, t_{DS} are measured form the earlier of $\overline{CE}$ or $\overline{WE}$ going high.

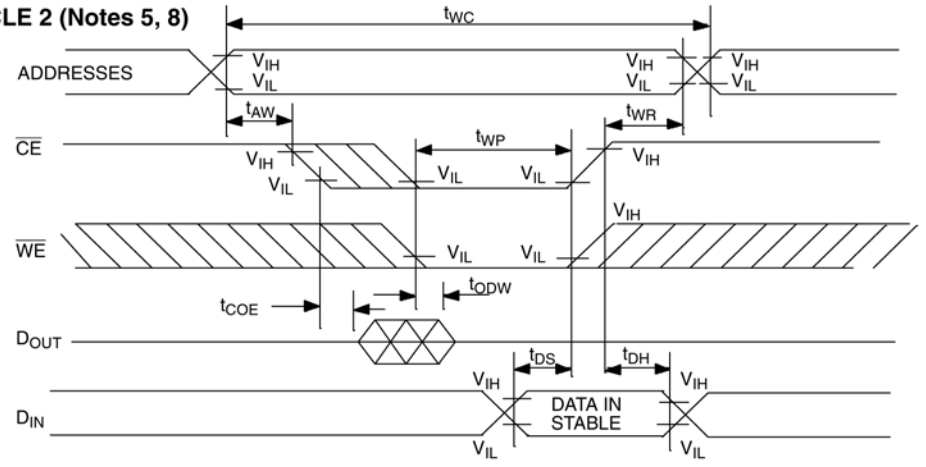
READ CYCLE (Note 4)



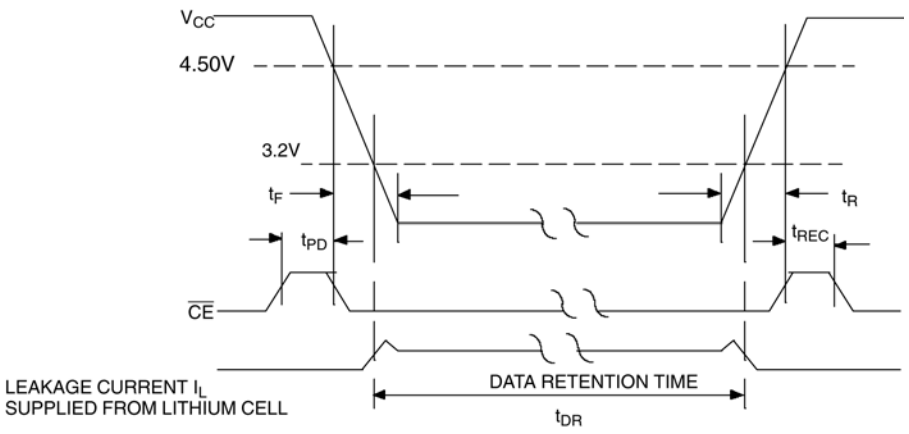
WRITE CYCLE 1 (Notes 5, 6, 7)



WRITE CYCLE 2 (Notes 5, 8)



POWER-DOWN/POWER-UP CONDITION



POWER-DOWN/POWER-UP TIMING

(T_A = 0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CE}$ at V_{IH} Before Power-Down	t_{PD}	(Note 9)	0			µs
V_{CC} Slew from 4.5V to 0 ($\overline{CE}$ at V_{IH})	t_F		100			µs
V_{CC} Slew from 0 to 4.5V ($\overline{CE}$ at V_{IH})	t_R		0			µs
$\overline{CE}$ at V_{IH} After Power-Up	t_{REC}	(Note 9)	2		125	ms

(T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Expected Data Retention Time	t_{DR}	(Note 10)	5			years

WARNING: Under no circumstances are negative undershoots of any amplitude allowed when the device is in battery-backup mode.

Note 4: $\overline{WE}$ is high for a read cycle.

Note 5: $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during a write cycle, the output buffers remain in a high-impedance state.

Note 6: If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ high transition in Write Cycle 1, that output buffers remain in a high-impedance state in this period.

Note 7: If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition in Write Cycle 1, the output buffers remain in a high-impedance state in this period.

Note 8: If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the CE low transition, the output buffers remain in a high-impedance state in this period.

Note 9: Removing and installing the cartridge with power applied may disturb data.

Note 10: Each DS1217M I smarked with a 4-digit code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected t_{DR} is defined as starting at the date of manufacture. This parameter is assured by component selection, process control, and design. It is not measured directly during production testing.

DC TEST CONDITIONS

Outputs Open
t Cycle = 250ns
All voltages are referenced to ground.

AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate
Input Pulse Levels: 0 to 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5ns

DETAILED DESCRIPTION

Read Mode

The DS1217M executes a read cycle whenever $\overline{WE}$ (write enable) is inactive (high) and $\overline{CE}$ (cartridge enable) is active (low). The unique address specified by the address inputs (A0–A14) defines which byte of data is to be accessed. Valid data will be available to the eight data I/O pins within t_{ACC} (access time) after the last address input signal is stable, provided that $\overline{CE}$ (cartridge enable) and $\overline{OE}$ (output enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ times are not satisfied, then data access must be measured from the late occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{CO} for $\overline{CE}$ or t_{OE} for $\overline{OE}$ rather than address access. Read cycles can only occur when V_{CC} is greater than 4.5V. When V_{CC} is less than 4.5V, the memory is inhibited and all accesses are ignored.

Write Mode

The DS1217M is in the write mode whenever both the $\overline{WE}$ and $\overline{CE}$ signals are in the active (low) state after address inputs are stable. The last occurring falling edge of either $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the first rising edge of either $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time (t_{WR}) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output bus has been enabled ($\overline{CE}$ and $\overline{OE}$ active), then $\overline{WE}$ will disable the outputs in t_{ODW} from its falling edge. Write cycles can only occur when V_{CC} is greater than 4.5 V. When V_{CC} is less than 4.5Vs, the memory is write-protected.

Data Retention Mode

The nonvolatile cartridge provides full functional capability for V_{CC} greater than 4.5V and guarantees write protection for V_{CC} less than 4.5V. Data is maintained in the absence of V_{CC} without any additional support circuitry. The DS1217M constantly monitors V_{CC}. Should the supply voltage decay, the RAM is automatically write-protected below 4.5V. As V_{CC} falls below approximately 3.0V, the power switching circuit connects a lithium energy source to RAM to retain data. During power-up, when V_{CC} rises above approximately 3.0V, the power switching circuit connects the external V_{CC} to the RAM and disconnects the lithium energy source. Normal RAM operation can resume after V_{CC} exceeds 4.5V.

The DS1217M checks battery status to warn of potential data loss. Each time that V_{CC} power is restored to the cartridge, the battery voltage is checked with a precision comparator. If the battery supply is less than 2.0V, the second memory cycle is inhibited. Battery status can, therefore, be determined by performing a read cycle after power-up to any location in memory, recording that memory location content. A subsequent write cycle can then be executed to the same memory location, altering data. If the next read cycle fails to verify the written data, the contents of the memory are questionable.

In many applications, data integrity is paramount. The cartridge thus has redundant batteries and an internal isolation switch that provides for the connection of two batteries. During battery backup time, the battery with the highest voltage is selected for use. If one battery fails, the other will automatically take over. The switch between batteries is transparent to the user. A battery status warning will occur only if both batteries are less than 2.0V.

Bank Switching

Bank switching is accomplished via address lines A8, A9, A10, and A11. Initially, on power-up all banks are deselected so that multiple cartridges can reside on a common bus. Bank switching requires that a predefined pattern of 64 bits is matched by sequencing 4 address inputs (A8 through A11) 16 times while ignoring all other address inputs. Prior to entering the 64-bit pattern, which will set the band switch, a read cycle of 1111 (address

inputs A8 through A11) must be executed to guarantee that pattern entry starts with the first set of 3 bits. Each set of address inputs is entered into the DS1217M by executing read cycles. The first 11 cycles must match the exact bit pattern as shown in Table 2. The last five cycles must match the exact bit pattern for addresses A9, A10, and A11. However, address line 8 defines which of the 16 banks is to be enabled, or all banks are deselected, as per Table 3. Switching from one bank to another occurs as the last of the 16 read cycles is completed. A single bank is selected at any one time. A selected bank will remain active until a new bank is selected, all banks are deselected, or until power is lost. (See the DS1222 BankSwitch Chip data sheet for more detail.)

Remote Connection through a Ribbon Cable

Existing systems that contain 28-pin bytewide sockets can be retrofitted using a 28-pin DIP plug. The DIP plug, AMP Part Number 746616-2, can be inserted into the 28-pin site after the memory is removed. Connection to the cartridge is accomplished via a 28-pin cable connected to a 30-contact card edge connector, AMP Part Number 499188-4. The 28-pin ribbon cable must be right justified, such that positions A1 and B1 are left disconnected. For applications where the cartridge is installed or removed with power applied, both ground contacts (A1 and B1) on the card edge connector should be grounded to further enhance data integrity. Access time push-out may occur as the distance between the cartridge and the driving circuitry is increased.

Table 1. Cartridge Numbering

PART	DENSITY	NO. OF BANKS
DS1217M 1/2-25	64kB x 8	2
DS1217M 1-25	128kB x 8	4
DS1217M 2-25	256kB x 8	8
DS1217M 3-25	384kB x 8	12
DS1217M 4-25	512kB x 8	16

Table 2. Address Input Pattern

ADDRESS INPUTS	BIT SEQUENCE															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A8	1	0	1	0	0	0	1	1	0	1	0	X	X	X	X	X
A9	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1
A10	1	0	1	0	0	0	1	1	0	1	0	1	1	1	0	0
A11	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	1

X = See Table 3

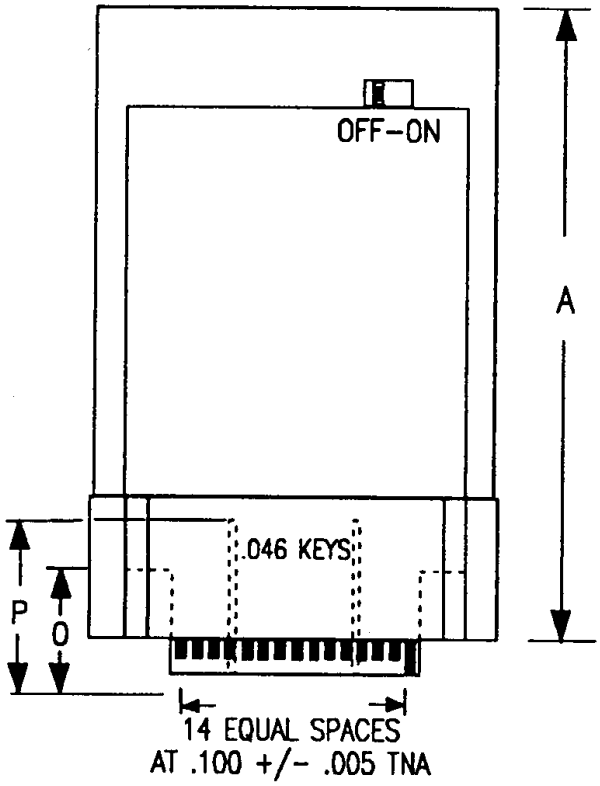
Table 3. Bank Select Table

BANK	A8 BIT SEQUENCE				
SELECTED	11	12	13	14	15
BANKS OFF	0	X	X	X	X
BANK 0	X	0	0	0	0
BANK 1	1	0	0	0	1
BANK 2	1	0	0	1	0
BANK 3	1	0	0	1	1
BANK 4	1	0	1	0	0
BANK 5	1	0	1	0	1
BANK 6	1	0	1	1	0

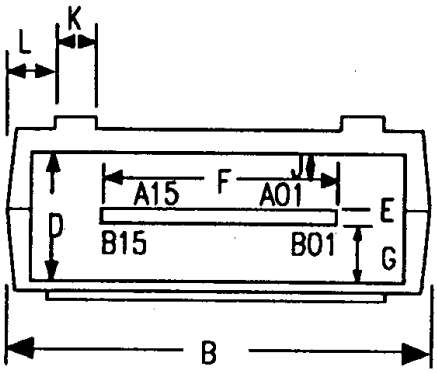
BANK	A8 BIT SEQUENCE				
BANK 7	1	0	1	1	1
BANK 8	1	1	0	0	0
BANK 9	1	1	0	0	1
BANK 10	1	1	0	1	0
BANK 11	1	1	0	1	1
BANK 12	1	1	1	0	0
BANK 13	1	1	1	0	1
BANK 14	1	1	1	1	0
BANK 15	1	1	1	1	1

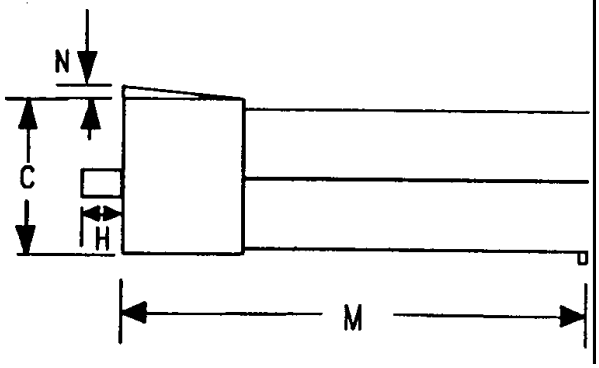
PACKAGE INFORMATION

For the latest package outline information, go to **www.maxim-ic.com/DallasPackInfo**.



DIM.	INCHES	
	MIN	MAX.
A	3.020	3.040
B	2.280	2.300
C	.600	.630
D	.440	.460
E	.060	.065
F	1.590	1.607
G	.220	.250
H	.115	.135
J	.115	.135
K	.115	.135
L	.140	.160
M	1.760	1.790
N	.040	.060
O	.039	.405
P	.405	.425





Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600